FACULTY OF SCIENCE
M. Sc. III – Semester Examination, January 2018

Subject: Physics
(Specialization: Electronics Instrumentation)

Paper – IV (A)
Digital Logic Circuits

Time: 3 Hours

Max. Marks: 80

Note: Answer all questions from Part–A and Part–B. Each question carries 4 marks in Part–A and 12 marks in Part – B.

PART – A (8 x 4 = 32 Marks)
(Short Answer Type)

1. Simplify the following Boolean function in product of sums.
   \[ F(A, B, C, D) = \Sigma (0, 1, 2, 5, 8, 9, 10) \]
2. Explain the binary subtraction process with an example.
3. Draw the circuit of NOR gate latch and explain.
4. Explain the decoding of a counter.
5. What are the TTL characteristics?
6. Draw the circuit of 8 to 1 multiplexer and explain.
7. Describe dynamic RAM structure and its operation.
8. Explain the significance of VHDL.

PART – B (4 x 12 = 48 Marks)
(Essay Answer Type)

9. (a) Discuss the simplification of Boolean function using four variable karnaugh map with an example.

   OR

   (b) Draw the circuit diagram of a BCD adder and explain its operation.

10. (a) Draw the logic diagram of a left to right shift register and explain.

    OR

    (b) Draw the logic diagram of IC asynchronous down counter and explain.

11. (a) Discuss the CMOS logic and its characteristics.

    OR

    (b) Discuss the magnitude comparator and code converter with necessary diagrams.

12. (a) Distinguish between static RAM and dynamic RAM. Draw the diagram of a 4 x 4 RAM and explain.

    OR

    (b) Explain the significance of VHDL and discuss VHDL syntaxes. Libraries and packages.